

# SARASWATI MAHILA MAHAVIDHYALAYA, PALWAL

## LESSON-PLAN

Class: BCA IST YEAR

Semester: Even

Subject: LOGICAL ORGANISATION OF COMPUTER-II

Session: 2021-22

Lecture Number	TOPIC
	<b>UNIT 1: SEQUENTIAL LOGIC</b>
L 1-20	sequential Logic basic introduction
	Difference between Sequential and Combinational Logic
	Characteristics of sequential logic
	Flip-Flops basic introduction
	Characteristics of flip-flops
	Clocked RS flip flop and excitation table
	Continued...
	D type
	Continue.
	JK flip flop
	Continue.
	T type flip flop
	Doubts taken on latch working of SR flip flop
	MasterSlave flip-flops
Difference between D and T type Flip Flop	

	<b>Continue..</b>
	<b>Flash Memory</b>
	<b>Doubt class</b>
	<b>Continue...</b>
	<b>I/O Devices and their controllers.</b>
	<b>Presentation on i/o Devices</b>
	<b>Continue.</b>
	<b>State Table of SR flip flop</b>
	<b>Continue.....</b>
	<b>Continue.....</b>
	<b>state diagram</b>
	<b>state equations.</b>
	<b>Continue.</b>
	<b>Flip-flop excitation tables</b>
	<b>UNIT 2: SEQUENTIAL CIRCUITS</b>
<b>L 21-40</b>	<b>Designing registers – Serial Input Serial Output (SISO), Serial Input Parallel Output (SIPO), Parallel Input Serial Output (PISO), Parallel Input Parallel Output (PIPO)</b>
	<b>Continue.....</b>
	<b>Continue.....</b>
	<b>Test on SR and JK FLIP - FLOP</b>
	<b>Discussed Doubts on JK and SR</b>

	shift registers.
	<b>Designing counters – Asynchronous and Synchronous Binary Counters</b>
	Continue.
	<b>Modulo-N Counters</b>
	Continue.
	<b>Up-Down Counters</b>
	Continue...
	<b>CLASS TEST</b>
	<b>UNIT 3: MEMORY DEVICES</b>
<b>L 40-60</b>	<b>Memory Parameters</b>
	<b>Semiconductor RAM</b>
	Continue....
	<b>ROM and types of ROM</b>
	<b>Magnetic and Optical Storage devices</b>
	Continue...
	<b>UNIT 4: INSTRUCTION DESIGN</b>
<b>L 60-80</b>	<b>I/O Organization</b>
	<b>Machine instruction</b>
	<b>Instruction set selection</b>
	<b>Instruction cycle</b>
	<b>Instruction Format</b>

	<b>Addressing Modes</b>
	<b>I/O Interface</b>
	<b>Interrupt structure</b>
	<b>CONTINUE...</b>
	<b>Program-controlled Interrupt-controlled &amp; DMA transfer</b>
	<b>CONTINUE...</b>
	<b>DOUBT CLASS</b>
	<b>ORAL TEST ON ADDRESSING MODE</b>
	<b>I/O Channels</b>
	<b>IOP.</b>